REMARKS

Currently, Claims 1-13 are pending in the application. Of these, Claims 11-13 have been withdrawn as being directed to a non-elected invention. Claims 14 and 15 have been added. Consideration of Claims 1-10, 14, and 15 is respectfully requested.

The Restriction Requirement and Election

Restriction to one of the following inventions is required under 35 U.S.C. § 121:

I. Claims 11-13, drawn to a multi-layer printed circuit board, and

II. Claims 1-10, drawn to a method of manufacture.

Applicants affirm the election of Claims 1-10, without traverse, for prosecution in this application. Claims 11-13 have been canceled without prejudice to file in a divisional application.

The Rejection of Claims 1, 4, 5, 7, and 9 Under 35 U.S.C. § 102(b)

Claims 1, 4, 5, 7, and 9 are rejected under 35 U.S.C. § 102(b) as purportedly being anticipated by applicants' admitted prior art (at present specification page 1, line 20, through page 10; Figs. 1-4).

Applicants respectfully disagree. Anticipation requires that the prior art exactly describe the claimed invention. Claim 1 recites in step (E): "forming circuit patterns on the outermost layers of a board *obtained by pressing the circuit layers and the insulating layers*." Using Fig. 8 to illustrate this embodiment, step (E) refers to forming circuit patterns on the uppermost and lowermost circuit layers 506b and 506c only after the circuit layers and insulating layers are pressed into a circuit board. This is because, in one embodiment of the invention, the via holes formed in the circuit layers 506b and 506c are not completely filled with plating as taught in the prior art. Compare the circuit layer of Fig. 1c (prior art) with the circuit layer of Fig. 5c. The via holes 504 in the circuit layers have openings despite being plated with copper. This allows the conductive paste from the insulating layers to flow into these openings. Because the conductive paste may overflow the surface of the circuit layers, a buffing step may be required. Because

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buffing the surface of the circuit layer may damage circuit patterns on the circuit layer, it is preferable to form the circuit patterns on the outermost circuit layers of the circuit board after the pressing step to determine whether a buffing step may be needed. If the outermost circuit patterns are formed before the pressing step, the buffing step to remove the conductive paste may result in damage to the outermost circuit layers.

At least, the aspect of pressing the arranged circuit and insulating layers and forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers is not described in applicants' description of the prior art.

In direct contrast to Claim 1, the prior art described on page 1, line 20, through page 10 and Figures 1, 3, and 4 has circuit patterns formed on the outermost circuit layers before pressing; therefore, the description of the prior art in the specification does not meet the limitations in Claim 1. Figure 3 shows the uppermost circuit layer 106a, and the lowermost circuit layer 106c having circuit patterns formed on the outermost surfaces. This is supported by the specification on page 1, line 23, through page 6, line 2, wherein it is stated "a circuit layer 106 (of Figure 1d) obtained by the above-described process serves as circuit layers 106a, 106b, and 106c of a multi-layer printed circuit board manufactured by a parallel or a batch stacking method, as shown in Figure 3." (Parenthetical Added.) Therefore, applicants describe that the conventional process is to provide circuit patterns on both sides of the uppermost and lowermost circuit layers. In direct contrast, Claim 1 specifically states that circuit patterns are formed on the outermost layers of a board *obtained by pressing the circuit layers and the insulating layers*. This means forming circuit patterns on the outermost layers of the circuit board that is created by pressing the circuit layers and the insulating layers. Because the description of the prior art refers to forming double-sided circuit layers as the uppermost and lowermost circuit layers in a circuit board, applicants' description of the prior art fails to anticipate Claim 1. Anticipation requires that every limitation be described either inherently or explicitly. Accordingly, for at least the reasons provided above, applicants have not admitted to

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the method of Claim 1 being prior art. Furthermore, Claims 4, 5, 7, and 9 are dependent from Claim 1; therefore, these claims are also not anticipated.

For the above-described reasons, applicants respectfully request withdrawal of the rejection of Claims 1, 4, 5, 7, and 9.

The Rejection of Claims 1, 3-5, and 7-10 Under 35 U.S.C. § 102(e)

Claims 1, 3-5, and 7-10 are rejected under 35 U.S.C. § 102(e) as purportedly being anticipated by Kim et al. (2004/0194303).

Applicants respectfully disagree. For a reference to be anticipatory, the reference must exactly describe the claimed invention.

Kim et al. describes a process whereby double-sided circuit layers are used as the uppermost and lowermost circuit layers that are then arranged and pressed with alternating insulating layers. Therefore, Kim et al. does not describe a process whereby "forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers" occurs after pressing the arranged circuit and insulating layers. At page 5, paragraph [0101], Kim et al. states: "the multi-layered PCB according to the present invention is structured such that a plurality of double-sided PCBs are continuously layered while insulating layers are inserted between the double-sided PCBs." See also Figure 7 of Kim showing the uppermost circuit layer 306a, and the lowermost circuit layer 306c having a circuit pattern formed on the outermost side before the pressing step.

For a reference to be anticipatory, the reference must exactly describe the claimed invention. Because Kim et al. does not, at least, describe "pressing the arranged circuit and insulating layers; and forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers," the reference is not anticipatory. Furthermore, Claims 3-5 and 7-10 depend directly from Claim 1; therefore, Claims 3-5, and 7-10 are also not anticipated by Kim.

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Accordingly, applicants respectfully request the withdrawal of the rejection of Claims 1, 3-5, and 7-10.

The Rejection of Claim 6 Under 35 U.S.C. § 103(a)

Claim 6 is rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over Kim et al. (2004/0194303) or applicants' admitted prior art, taken with DiFranco (U.S. Patent No. 5,332,486).

Applicants respectfully disagree. For a *prima facie* case of obviousness, first there must either be a suggestion or a motivation, either in the prior art or in the knowledge generally available, to modify a reference or to combine references. Second, there must be a reasonable expectation of success, and, third, all the claim limitations must be taught or suggested by the prior art references.

As an initial matter, applicants believe that the Examiner has recited the incorrect secondary reference. Instead of DiFranco (U.S. Patent No. 5,332,486), applicants believe the correct reference is Hirose et al. (U.S. Patent No. 6,613,986). Applicants will, therefore, respond assuming Hirose et al. is the correct secondary reference.

The Examiner states:

> Kim and Applicant's admitted prior art lack mentioning buffing a portion of the conductive paste, flowing out from the via holes of the outmost layer, so as to remove the protruding portion of the conductive paste, after the step (C).
>
> However, DiFranco teaches (at Figs 24C-25B, col 29, lines 10-22; col 28, line 58 through col 29; Figs 1A-2D; col 16, lines 46-55) to buffing a portion of the conductive paste, flowing out from the via holes of the outmost layer, so as to remove the protruding portion of the conductive paste.

Based on this, the Examiner concludes that

> it would have been obvious to one of ordinary skill in the art at the time the invention was made to manufacture the printed circuit board of Kim or Applicant's admitted prior art by buffing a portion of the conductive paste flowing out from the via holes of the outmost layer, as taught by DiFranco. This is because of the desirability to remove the unwanted protruding portion of the conductive past [sic] flowing out from the via holes.

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Claim 6 recites "buffing a portion of the conductive paste, flowing out from the via holes of the outermost layer, so as to remove the protruding portion of the conductive paste, after the step (D)." From Claim 1, step (D) is "pressing the arranged circuit and insulating layers." Therefore, the buffing process recited in Claim 6 is performed on a circuit board after being created by pressing arranged circuit and insulating layers. In Hirose et al., Figures 24C-25B, and 24E in particular, refer to a single copper clad laminate 30a including a substrate 30 with copper foils 32 laminated on both sides thereof as a starting material. See Col. 29, lines 15-22. Figures 1A-2D of Hirose et al. also refer to a single circuit layer, before pressing. Therefore, Hirose et al. does not describe buffing the outermost layer, after pressing.

Furthermore, the conductive paste flowing out from the via holes of the outermost layer of both Kim et al. and applicants' description of the prior art is impossible. In both Kim and applicants' description of the prior art, the circuit layers have via holes completely filled with electroplating that do not allow for a conductive paste to fill the via holes. Therefore, buffing is an unnecessary step in both Kim and the described prior art. For example, see Figure 3C of Kim et al. and page 4, paragraph [0069], describing that plated layers 305 are formed on both sides of the copper clad laminate 301, and the via holes 304 are plugged by copper. Applicants' description of the prior art similarly describes circuit layers plugged with copper, and therefore cannot admit a conductive paste into the via holes, thereby making the buffing process unnecessary. For example, please see Figure 1c, and the application at page 5, lines 8-14, wherein is stated, "upper and lower surfaces of the copper stack plate 101 and inner walls of the via holes 104 are plated by electro-plating and electroless-plating. Thereby, as shown in FIG. 1c, plating layers 105 are respectively formed on the upper and lower surfaces of the copper stack plate 101, the via holes 104 are filled by plating."

Therefore, there is no suggestion or motivation to combine Hirose et al., either with Kim et al. or the described prior art, because a conductive paste is not introduced into the via holes of circuit layers in either Kim or applicants' description of the prior art; therefore, a buffing

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step in Kim or the described prior art is pointless. Even assuming that the combination is attempted, the combination does not result in the claimed invention of Claim 6, since Hirose et al., at least, does not teach or suggest buffing after pressing. Furthermore, because the via holes of circuit layers in Kim et al. and the description of the prior art are completely plugged with copper, the conductive paste cannot be introduced within via holes of the circuit layers; therefore, the combination of Hirose et al. with Kim et al. or the described prior art cannot reasonably be expected to succeed. Finally, neither Kim et al., Hirose et al., nor the described prior art teaches or suggests all the claim limitations, including, at least, the combination of steps of pressing the arranged circuit and insulating layers and forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers. Accordingly, the Examiner has not set forth a tenable *prima facie* case of obviousness.

Therefore, applicants respectfully request withdrawal of the rejection of Claim 6.

Allowable Subject Matter

Applicants acknowledge with appreciation the indication of allowable subject matter in Claim 2.

New Claims 14-17

Claims 14-17 have been added. Applicants submit that none of Claims 14-17 are anticipated or rendered obvious by the prior art of record.

Amended Claim 6

Claim 6 has been amended to correct typographical errors, including referencing the incorrect step (C) instead of (D), correcting the misspelling of "outmost" to "outermost," and changing "layer" to "layers."

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CONCLUSION

In view of the foregoing remarks, applicants respectfully submit that Claims 1-10 and 14-17 are in condition for allowance. If the Examiner has any further questions or comments, the Examiner is invited to contact the applicants' attorney at the number provided below.

Respectfully submitted,

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Date: October 3, 2005

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